WHAT IS CLAIMED IS:

1. A method for forming bit line and storage node contacts for a dynamic random access device, the method comprising:

providing a substrate, the substrate having a bit line region and a capacitor contact region;

forming at least a first gate structure and a second gate structure overlying the substrate, the first gate structure including an overlying first cap, the second gate structure including an overlying second cap, the first gate structure being spaced by the bit line region to the second gate structure, the capacitor contact region being coupled to the first gate structure;

forming a conformal dielectric layer overlying the first gate structure, the second gate structure, the bit line region, and the capacitor contact region;

forming an interlayer dielectric material overlying the conformal dielectric layer;

planarizing the interlayer dielectric material;

forming a masking layer overlying the planarized interlayer dielectric material;

exposing a continuous common region within a portion of the planarized interlayer dielectric material overlying a portion of the first gate structure, a portion of the second gate structure, a portion of the bit line region, and a portion of the capacitor contact region;

performing a first etching process to remove the exposed portion of the planarized interlayer dielectric layer;

performing a second etching process to remove a portion of the conformal dielectric layer on the bit line region and to remove a portion of the conformal dielectric layer on the capacitor contact region while using other portions of the conformal layer as a mask to prevent a portion of the first gate structure and a portion of the second gate structure from being exposed; depositing a polysilicon fill material within the continuous common region and overlying the bit line region, the capacitor contact region, the first gate structure, and the second gate structure to cover portions of the bit line region, the capacitor contact region, the first gate structure, and the second gate structure to a predetermined thickness;

planarizing the polysilicon fill material to reduce the predetermined thickness and to simultaneously reduce a thickness of a portion of the interlayer dielectric material;

continuing the planarization of the polysilicon fill material and the interlayer dielectric material; and

exposing a portion of the first gate structure and a portion of the second gate structure while leaving portions of the polysilicon fill material on the portion of the capacitor contact region and the portion of the bit line region, whereupon the polysilicon fill material on the portion of the capacitor contact region is isolated from the polysilicon fill material on the portion of the bit line region.

2. The method of claim 1 wherein the first gate structure including an overlying first tungsten silicide layer and the second gate structure including an overlying second tungsten silicide layer.

3. The method of claim 1 wherein the conformal dielectric layer is silicon nitride.

4. The method of claim 1 wherein the planarizing includes a chemical mechanical polishing process and/or an etch back process.

5. The method of claim 1 wherein the wherein the polysilicon fill material is an in-situ doped polysilicon material or an amorphous silicon material or an in-situ-doped amorphous silicon material or a polysilicon material or a doped polysilicon material.

6. The method of claim 1 wherein the wherein the polysilicon fill material in the portion capacitor contact region is electrically isolated from the first gate structure and the second gate structure and the polysilicon fill material in the portion of the bit line region is electrically isolated from the first gate structure and the second gate structure.

7. The method of claim 1 wherein the continuous common region is shaped as an "I" configuration.

8. The method of claim 1 wherein the continuous common region is shaped as a "T" configuration.

9. The method of claim 1 wherein the first gate structure and the second gate structure are spaced by the bit line region, the space being about 0.135 microns and less.

10. The method of claim 1 wherein the first gate structure is characterized by a design dimension of 0.13 micron and less the second gate structure is characterized by a design dimension of 0.13 micron and less.

11. A method for forming a self aligned contact region for a dynamic random access memory device, the method comprising:

providing a semiconductor substrate, the semiconductor substrate having a cell region and a peripheral region;

forming at least a first gate structure, a second gate structure, a third gate structure, and a fourth gate structure in the cell region and forming a gate structure in the peripheral region, the first gate structure including an overlying first cap, the second gate structure including an overlying second cap, the third gate structure including an overlying third cap structure, the fourth gate structure including an overlying fourth cap structure, the second gate structure being spaced by a bit line region to the third gate structure, the first gate structure being spaced by a first capacitor contact region to the second gate structure, the third gate structure being spaced by a second capacitor contact region to the fourth gate structure;

forming a conformal dielectric layer overlying the first gate structure, the second gate structure, the third gate structure, the fourth gate structure, the bit line region, the first capacitor contact region, and the second capacitor contact region in the cell region and the gate structure in the peripheral region;

forming an interlayer dielectric material overlying the conformal dielectric layer;

planarizing the interlayer dielectric material;

forming a masking layer overlying the planarized interlayer dielectric material;

exposing a continuous common region within a portion of the planarized interlayer dielectric material overlying the first gate structure, the second gate structure, the third gate structure, the fourth gate structure, the bit line region, the first capacitor contact region, and the second capacitor contact region while maintaining the planarized interlayer dielectric material overlying the gate structure in the peripheral region;

performing an etching process to remove the exposed portion of the planarized interlayer dielectric layer in the continuous common region to expose the bit line contact, the

first capacitor contact region, and the second capacitor contact region while using portions of the conformal layer as a mask to prevent any conductive portions of the first gate structure, the second gate structure, the third gate structure, and the fourth gate structure from being exposed;

depositing a polysilicon fill material within the continuous common region and overlying the bit line region, the first capacitor contact region, and the second capacitor region, the first gate structure, the second gate structure, the third gate structure, and the fourth gate structure to a predetermined thickness;

planarizing the polysilicon fill material to reduce the predetermined thickness and to simultaneously reduce a thickness of a portion of the interlayer dielectric material to a vicinity of an upper region of the first gate structure, the second gate structure, the third gate structure, the fourth gate structure, and the gate structure;

continuing the planarization of the polysilicon fill material and the interlayer dielectric material; and

exposing a portion of the first gate structure, a portion of the second gate structure, a portion of the third gate structure, a portion of the fourth gate structure, and a portion of the gate structure while leaving portions of the polysilicon fill material on the bit line region, the first capacitor contact region and the second capacitor contact region, whereupon the polysilicon fill material on the first capacitor contact region is isolated from the polysilicon fill material on the bit line region and the polysilicon fill material on the second capacitor contact region is isolated from the polysilicon fill material on the bit line region.

12. The method of claim 11 wherein the first gate structure including an overlying first tungsten silicide layer and the second gate structure including an overlying second tungsten silicide layer, the third gate structure including an overlying third tungsten layer, the fourth gate structure including an overlying fourth tungsten layer, and the gate structure including an overlying tungsten layer.

13. The method of claim 11 wherein the conformal dielectric layer comprises silicon nitride.

14. The method of claim 11 wherein the planarizing includes a chemical mechanical polishing process and/or an etch back process.

15. The method of claim 11 wherein the wherein the polysilicon fill material is an in-situ doped polysilicon material or an amorphous silicon material or an in-situ-doped amorphous silicon material or a polysilicon material or a doped polysilicon material.

16. The method of claim 11 wherein the wherein the polysilicon fill material in the first capacitor contact region is electrically isolated from the first gate structure and the second gate structure; wherein the polysilicon fill material in the bit line region is electrically isolated from the second gate structure and the third gate structure; and wherein the second capacitor contact region is electrically isolated from the third gate structure and the fourth gate structure.

17. The method of claim 11 wherein the continuous common region is shaped as an "I" configuration.

18. The method of claim 11 wherein the continuous common region is shaped as a "T" configuration.

19. The method of claim 11 wherein the second gate structure and the third gate structure are spaced by the bit line region, the space being about 0.135 microns and less; and wherein the first gate structure, the second gate structure, the third gate structure, and the fourth gate structure is characterized by a design dimension of 0.13 micron and less.